Register 12:

Always set to: 0001041c (normal operation, phase sync not used)

Register 11:

Always set to: 0061300b (reserved)

Register 10:

Calculate (8 bit result):

$$ADC\_CLKDIV = INT(\frac{\frac{f_{pfd}}{100000} - 2}{4} + 0.5)$$

Use ADC_EN=1 and ADC_CONV=1

Set to: 00c0000a + (ADC_CLKDIV<<6) + (ADC_CONV<<5) + (ADC_EN<<4) (ADC settings)

Register 9:

Calculate (8 bit result):

$$VCO\_Band\_Div = INT(\frac{f_{pfd}}{2400000} + 0.5)$$

Take:

$$ALC\_TO = INT(\frac{50\mu s \cdot f_{pfd}}{Timeout} + 0.5)$$

$$Lock\_TO = INT(\frac{20\mu s \cdot f_{pfd}}{Timeout} + 0.5)$$

ALC_TO = 30 (5 bit)

LOCK_TO = 12 (5 bit) → as ALC_TO = LOCK_TO x 2.5

Calculate (10 bit result):

$$Timeout = INT\left(\frac{50\mu s \cdot f_{pfd}MHz}{ALC\_TO} + 0.5\right) = INT(\frac{50\mu s \cdot f_{pfd}MHz}{30} + 0.5)$$

Set to: (VCO_Band_Div<<24) + (Timeout<<14) + (ALC_TO<<9) + (LOCK_TO<<4) + 9
(timeout settings)

Register 8:

Always set to: 102d0428 (reserved)

Register 7:

We take enough time for locking (still only a few µs) and we set the factional-N mode stuff…

Use: LE = 1, LD_CYC=3, LOLM=0, F_N_PREC=3, LDM=0

Set to: 10000007 + (LE<<25) + (LD_CYC <<8) + (LOLM<<7) + (F_N_PREC <<5) + (LDM<<4)
(lock settings)

Register 6:

GB=1 (Gated bleed to improve lock speed, only use with digital lock detect enabled)

NB=1 (Negative bleed recommended for frac-N applications)

FB=1 (use fundamental output from VCO)

Set RDIV that the VCO stays within 3.4…6.8GHz range

$$f_{out} = \frac{f_{vco}}{2^{RDIV}} \quad \rightarrow \quad RDIV = log2(\frac{f_{vco}}{f_{out}})$$

Set BC (bleed current) so that

$$\frac{4}{N} < \frac{I_{bleed}}{I_{CP}} < \frac{10}{N}$$

MTLD=1 (keep outputs muted until lock reached)

Enable RFB and/or RFA depending on what RF output to use (auxiliary B and/or main A)

Set PWR to 0…3 corresponding to -4…5dBm (steps of 3dBm) for output A

Set to: (GB<<30)|(NB<<29)|(FB<<24)|(RDIV<<21)|(BC<<13)|(MTLD<<11)|(RFB<<10)
|(RFA<<6)|(PWR<<4)|6

Register 5:

Always set to: 00800025 (reserved)

Register 4:

f_pfd must be <125MHz and is calculated as:

$$f_{pfd} = f_{ref} \cdot \frac{1 + D}{R \cdot (1 + T)}$$

Set MUXOUT = 6 (digital lock detect) for GB in register 6 to work

Set D = 0 (you may enable reference doubler to improve system noise performance)

Set T = 0 to disable reference divider (only needed if PFD gets >125MHz)

Set R = 1, we don’t need this (use this if requiring certain steps with simpler calculations)

Set DB = 1, we want double-buffering of the RF divider for an arbitrary f_out programming

Set CP = 2, this is the recommended (0.9mA setting for low spur)

Set RM = 1, RM=0 is recommended for any f_ref < 250MHz, but does not lock on my board…

Set LS = 1, we use a 3.3V interface

Set PDP = 1, as we have a passive (non-inverting) loop filter

Set PD = 0 for normal operation (IC not in power down)

Set CPT = 0 for normal operation (CP not in tristate)

Set RES = 0 for normal operation (IC not in reset)

Set to: (MUXOUT<<27)|(D<26)|(T<<25)|(R<<15)|(DB<<14)|(CP<<10)|(RM<<9)| (LS<<8)|
(PDP<<7)|(PD<<6)|(CPT<<5)|(RES<<4)|4

Register 3:

Always set to 00000003, we don't use phase adjustments and resynchronisation

Register 2, 1, 0:

This registers are used to calculate N for the mapping of f_pfd to f_out:

$$f_{out} = f_{pfd} \cdot N$$

FRAC2, MOD2, FRAC1, INT forms the formula:

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{16{,}777{,}216}$$

INT: 23…32767 or 75…65535 (16bit - 4/5 or 8/9)

FRAC1: 1…16777215 (24bit)

FRAC2: 0…16383 (14bit)

MOD2: 2…16383 (14bit)

Furthermore, we use a 4/5 prescaler and enable autocal:

PRE=0
ACAL=1

Set to: (FRAC2<<18)|(MOD2<<4)|2

(FRAC1<<4)|1

(ACAL<<21)|(PRE<<20)|(INT<<4)|0